

A GaN HEMT Class F Amplifier at 2 GHz with > 80 % PAE

David Schmelzer, *Student Member, IEEE*, and Stephen I. Long, *Senior Member, IEEE*
Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA, 93106, USA

Abstract — A Class F amplifier has been designed, fabricated, and tested using a GaN HEMT transistor and a hybrid PCB. The amplifier has a peak PAE of 85 % with an output power of 16.5 W. An output power and drain efficiency tradeoff, dependant on the drain impedance at the fundamental frequency due to the on-state resistance, is explored. A comparison between Class F and inverse F, given particular operating conditions for this device, are made.

Index Terms — Class F, Inverse F, GaN HEMT

I. INTRODUCTION

A Class F amplifier can achieve a theoretical 100% drain efficiency by wave shaping the intrinsic drain voltage and current waveforms [1]. When the amplifier is driven into saturation and the device is biased at cutoff, the voltage waveform is clipped and can be shaped like a square wave and the current waveform can be shaped like a half sine wave with proper harmonic terminations. The voltage and the current waveforms do not overlap, minimizing the power dissipation. The squared voltage waveform contains only odd harmonic frequencies. Ideally it must have all of the odd harmonics terminated with an open circuit at the intrinsic drain of the transistor. The half sine wave current waveform only contains even harmonics, and all the even harmonics need a short circuit termination for the harmonic current to flow through.

For an RF amplifier it is not practical to terminate an infinite number of harmonics. Raab has shown that most of the gain in efficiency due to wave shaping can be had with just the first few harmonics correctly terminated [1]. For example, with up to and including the fourth harmonic present and terminated correctly, the efficiency of an ideal amplifier can be as high as 86%.

Realistically, the efficiency of the amplifier is limited by the transistors drain-source capacitance, C_{ds} , and its on-state resistance, R_{on} , or knee voltage. C_{ds} is often difficult to absorb into a multiple harmonic matching network without compromising the ability to terminate higher harmonics. A device with a high f_{max} compared to the fundamental operating frequency is helpful to generate the higher order harmonics needed for waveshaping. In this respect, GaN HEMT transistors are good candidates for Class F amplifiers. GaN transistors have demonstrated a significantly higher power density (>10x) than their GaAs and Si counterparts [2], resulting in lower input and output capacitances for the same power output. They have higher peak operating voltages and consequently higher drain impedances at the operating frequency.

Several published reports have presented Class F amplifiers with PAEs up to 77% with GaAs transistors about the

operating frequency of 2 GHz. To the authors' knowledge, there has not been a published report of a Class F with greater than 10 W of power and 80% PAE in this frequency range. A Class E amplifier with the same GaN HEMT transistor has been demonstrated to have 85% PAE and 10 W output power by [3]. Implementing a Class F or inverse F amplifier with a GaN transistor is very promising because of the greater power output capability compared to a Class E amplifier using the same transistor. This paper demonstrates a successful Class F amplifier design using a GaN HEMT transistor.

II. DESIGN

The GaN HEMT devices on SiC substrate that were used in this amplifier, were provided by Cree and has a 3.6 mm gate periphery and has an estimated f_{max} of 40 GHz. The transistor has a breakdown voltage greater than 90 V. The amplifier was designed to maximize power added efficiency while maintaining a high output power for an operating frequency of 2 GHz.

A. Power and Efficiency

In [1], the calculations were based on an ideal amplifier with zero R_{on} , where the voltage across the drain is zero when the transistor is conducting. If the on-state resistance is included in the transistor model, there is a voltage drop, V_{min} , across the transistor when it is conducting. The peak voltage swing is reduced and the efficiency drops. The waveform factors, (1) and (2), derived in [1] to relate harmonic amplitudes and peak waveform values, can still be used but must include V_{min} .

$$V_{om} = \gamma_V (V_{DD} - V_{min}), V_{max} = \delta_V (V_{DD} - V_{min}) \quad (1) \text{ a,b}$$

$$I_{om} = \gamma_I I_{DC}, I_{max} = \delta_I I_{DC} \quad (2) \text{ a,b}$$

Continuing from (1) and (2), the output power, (3)a, and drain efficiency, (4), are found with a dependency on V_{min} . The intrinsic drain impedance, R_L , at the fundamental frequency is defined by (3)b. This is defined at the intrinsic drain, such that C_{ds} and other transistor parasitic elements are absorbed into the matching network that presents R_L . (3) and (4) show that increasing V_{DD} and minimizing V_{min} will maximize drain efficiency and output power.

$$P_{out} = \frac{V_{om}^2}{2R_L} = \frac{\gamma_V^2 V_{DD}^2}{2R_L} \left(1 - \frac{V_{min}}{V_{DD}}\right)^2, R_L = \frac{V_{om}}{I_{om}} \quad (3) \text{ a,b}$$

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$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\gamma_V \gamma_I}{2} \left(1 - \frac{V_{min}}{V_{DD}} \right) \quad (4)$$

With ideal drain waveforms, V_{min} is equal to (5) and it is inversely proportional to R_L . It is important to note that (5) is not correct for amplifiers with harmonic output networks limited to the 3rd harmonic or without maximally flat voltage waveforms. In this more realistic case, V_{min} is actually lower than (5) predicts because the peak current and the minimum voltage across the device do not coincide. Therefore (5) will over estimate the loss in efficiency and power output due to the on-state resistance of the device.

$$V_{min} = V_{DD} \left(1 + \frac{\gamma_I}{\delta_I \gamma_V} \frac{R_L}{R_{ON}} \right)^{-1} \quad (5)$$

The equations (3)-(5) do present the general trends for Class F and inverse F amplifiers. Drain efficiency increases as R_L is increased but at the expense of output power. Therefore, V_{DD} should be set so that the peak voltage is approximately equal to the breakdown voltage of the device to achieve the highest output power for a given efficiency determined by R_L .

B. Drain Impedance

Fig. 1 shows results of a harmonic balance simulation of the large signal GaN transistor model with the intrinsic drain ideally terminated with the 2nd, 3rd, and 4th harmonics. The transistor's input is optimally matched at the fundamental frequency, and the 2nd harmonic impedance is short circuited. All other higher order input harmonics in the simulation are terminated by 50 Ohms. The transistor's gate is biased at cutoff and the drain bias voltage is set to 40 V. The high breakdown voltage of the transistor allows for a trade off of power for efficiency by the choice of impedance. The graph displays the drain efficiency and output power at maximum PAE versus R_L . This simulation predicts best case performance since there are no passive network losses. The maximum drain efficiency observed in this simulation is 89.3% at the highest value of R_L . When the transistor is matched to a R_L larger than 150 Ohms there is an excessive loss in gain. The efficiency is higher than the predictions based on waveform analysis in [1] because the transistor generates quite a bit more harmonic content beyond the 4th harmonic. Even though these harmonics are not terminated optimally, they contribute to a higher than expected efficiency.

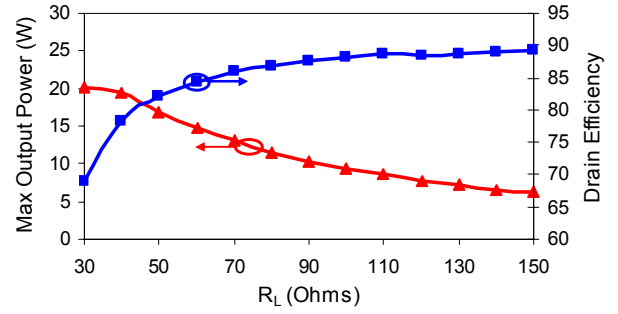


Fig. 1. Simulation results at 2 GHz of output power and drain efficiency at max PAE versus R_L .

C. Input Harmonic Matching

It has been observed in [4] that input matching network must have proper harmonic terminations to preserve a sinusoid drive at the gate due to the nonlinear C_{gs} . A simulation of a source pull for the second harmonic termination indicated that the Class F amplifier would have the highest PAE, 84 %, given second harmonic termination near a short circuit. Surprisingly, the impedance with the worst PAE of 35 % was only 16 degrees of phase difference from the optimum point. Therefore it was crucial to accurately model the second harmonic input termination presented to this transistor.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The output matching network must absorb C_{ds} and the interconnect inductance while providing the correct fundamental and harmonic resistances at the intrinsic drain of the transistor. It is beneficial if the matching network can be tuned to different values of R_L so the amplifier can be designed for different supply voltages, especially for GaN transistors which can be matched to a range of impedances due to the high breakdown voltage.

Fig. 2 illustrates a matching network that can accomplish this. Two separate bondwires are used at the drain pad and approximated by L_{bw} . This allows the bondwire inductance to be incorporated into the quarter-wave length drain bias transmission line giving the lowest even harmonic impedances at the drain. Z_2 , θ_2 and Z_3 can be tuned to absorb C_{ds} and L_{bw} and simultaneously present a real impedance at the fundamental, R_L , and a very high real impedance at the 3rd harmonic. Effectively, both matching networks terminate the 2nd, 3rd and 4th harmonics and some of the higher order even harmonics as well.

An intrinsic drain impedance of 70 Ohms was chosen for the design as it was a good tradeoff of efficiency and output power. Tuning the output matching network in Fig. 2 to a R_L equal to 70 Ohms resulted in 3rd harmonic impedance of about 400 Ohms. The 2nd harmonic impedance was about 0.5 Ohms and the 4th harmonic was about 0.7 Ohms.

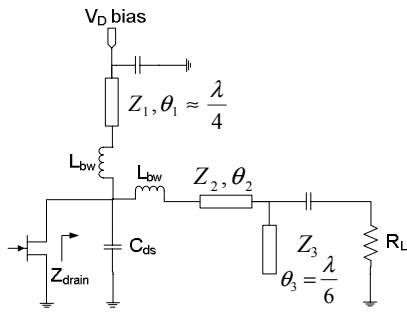


Fig. 2. The output matching network that presents approximately Z_{drain} to the intrinsic drain of the transistor

The output matching network topology is a particularly good fit for this GaN transistor with a C_{ds} of about 0.9 pF. The output matching network was capable of tuning R_L from 25 to 120 Ohms while maintaining a high 3rd harmonic impedance and realizable transmission line impedance.

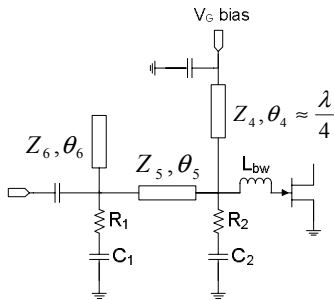


Fig. 3. The input matching network

An input matching network was synthesized, Fig. 3, that provides a second harmonic short and fundamental match. Two RC networks were added to provide stability. Stability was evaluated by a similar method used by [5], using an ideal circulator to determine an open loop transfer function of the amplifier and applying Nyquist criterion. This enabled stabilization with out excessive loss in gain.

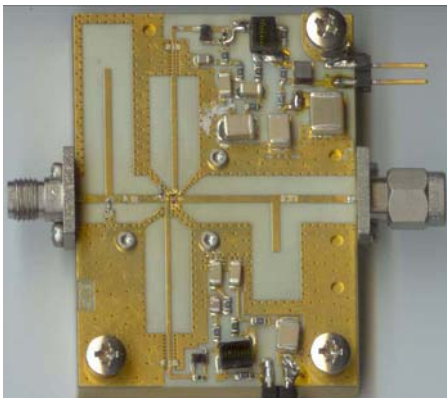


Fig. 4. Picture of Amplifier

The amplifier was constructed on a low loss printed circuit board substrate with gold plated traces mounted to a copper carrier. The GaN HEMT IC was directly mounted to the

copper carrier and used wirebond interconnects. Fig. 4 shows a picture of the amplifier.

The amplifier was tested at 2 GHz and the performance measured is in Fig. 5. Only the fundamental frequency component was measured for the results. The amplifier had a peak PAE of 85.5 % with an output power of 16.5 W with a drain bias voltage of 42.5 V. The peak gain was 15.8 dB, and it had a compressed gain a peak PAE of 13.0 dB. The peak drain efficiency was 91 %.

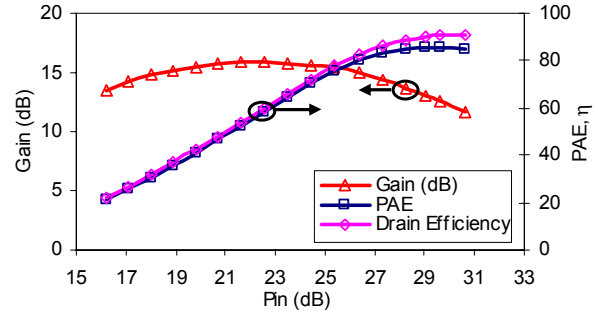


Fig. 5. Measured gain, PAE and drain efficiency at 2 GHz with 42.5 V drain bias

The measured performance of the amplifier at the peak PAE with respect to drain bias voltage is in Fig. 6. The peak PAE is above 80 % for drain voltages greater than 27V.

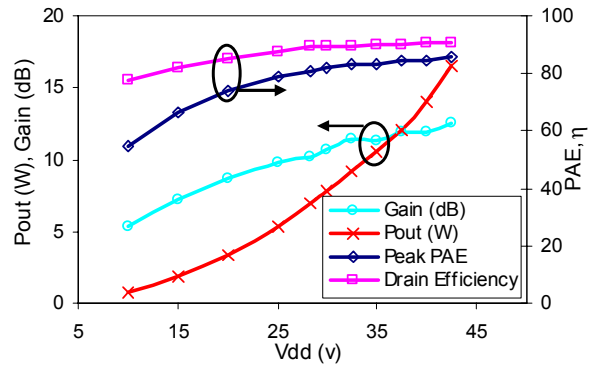


Fig. 6. Measured gain, output power, peak PAE and drain efficiency at 2 GHz with respect to drain voltage bias

IV. CLASS F AND INVERSE F

Since the introduction of the inverse Class F amplifier [6], several papers have stated its superiority to the Class F amplifier. An ultimate comparison can not be made, because one must consider the operating conditions and constraints. For instance, [7] demonstrated that an inverse F amplifier has a higher efficiency than a class F given that they are operating at the same drain bias and the peak voltage swing is less than the breakdown voltage.

If one would have to choose between the two amplifiers for a fixed device to maximize the PAE and output power, you would first need to consider the constraints the application presents. For instance, the drain bias needs to be fixed at a

particular voltage because the amplifier will be used in a mobile application. Alternatively, if the amplifier would be used in a base station, the only constraint could be the device's own operating limits and the selection of the bias would be unconstrained.

Using (3)-(5) and the waveform coefficients for a Class F and Class Inverse F found in [1], one can make an idealized comparison between the two. In the first case of a fixed drain bias, to compare drain efficiency at equal output powers, one must solve for R_L in for each amplifier as they are not equal. Qualitatively, the ratio of the efficiency of the F to the inverse F is equal to the inverse of the ratio of the DC currents. Since the inverse F will have a lower I_{DC} for the same drain bias, it will also have higher drain efficiency.

To truly maximize the output power and drain efficiency of an amplifier, one must lift the constraint of fixing the drain bias so that it can be scaled such that the voltage swing across the device is as large as possible. P_{out} and drain efficiency can be calculated using (3)-(5) after solving for R_L for a given peak voltage. The result is plotted in Fig. 6. The Class F amplifier will have higher drain efficiency for the same output power when the two amplifiers have the same peak output voltage.

Using the large signal model of the GaN device, the calculated result was compared with simulations of both configurations of amplifiers. The simulations consisted of the amplifiers with the 2nd and 3rd output harmonics ideally terminated. The 2nd input harmonic was optimally terminated as well. The fundamental intrinsic drain impedance was swept and the peak drain efficiency and output power were measured.

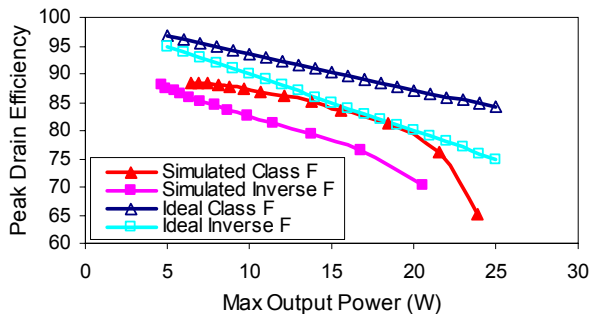


Fig. 6. Comparison of maximum drain efficiency vs. peak output power of Class F and Inverse F amplifiers with a constant peak voltage of 80V.

The simulation of the class F amplifier has higher drain efficiency because it has a lower I_{RMS} than the inverse F amplifier in this case. The power dissipated due to R_{on} is

about equal to the product of R_{on} and I_{RMS} . Comparing the simulations to the calculations in Fig. 6 we see good agreement in the slope and efficiency difference. If the calculations were to use the waveform factors that can be extracted from the simulations, they match quite well.

V. CONCLUSION

GaN transistors offer the potential for significant improvement in the performance of Class F amplifiers over their GaAs counter parts. Implementing the amplifier in a hybrid PCB technology facilitates easy matching of higher order harmonics and results in high power added efficiency. For a given device, a Class F amplifier should ideally have higher drain efficiency than an inverse F, when their peak voltages are equal.

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